

Start with Si substrate

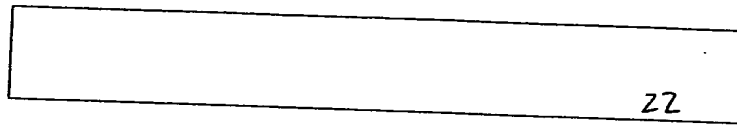


Fig. 1A

Form device isolation

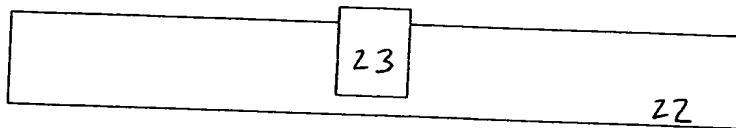


Fig. 1B

Gate oxidation

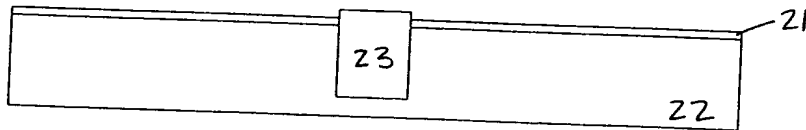


Fig. 1C

Deposit gate electrode material

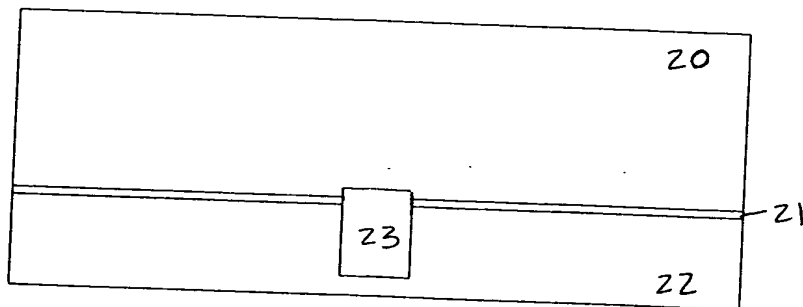


Fig. 2

Apply photoresist  
Pattern photoresist  
Hardmask open

patterned  
photoresist

Hard  
mask

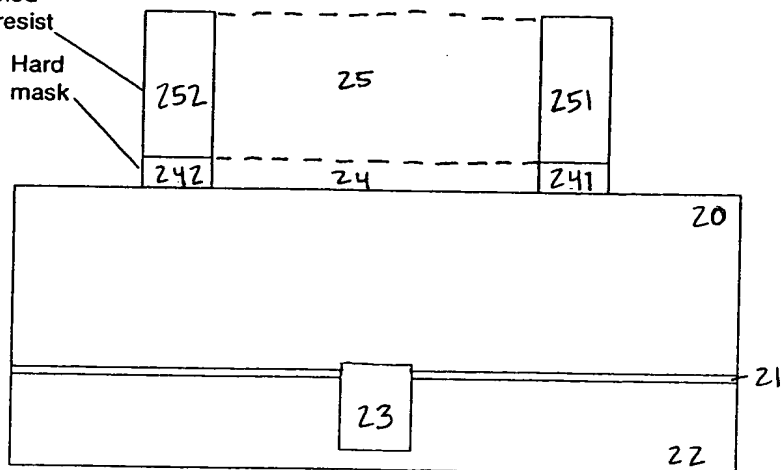


Fig. 3

Remove Photoresist  
Gate stack etch

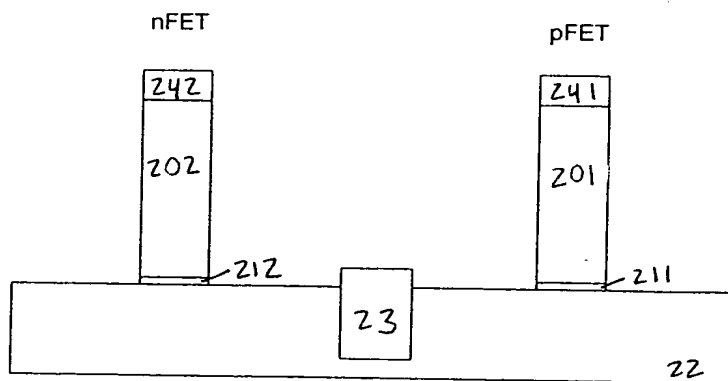
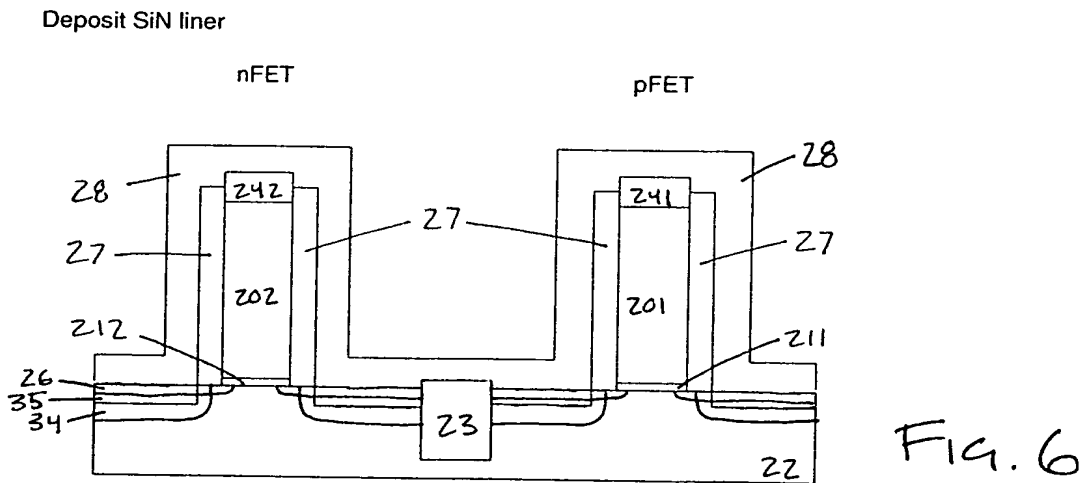
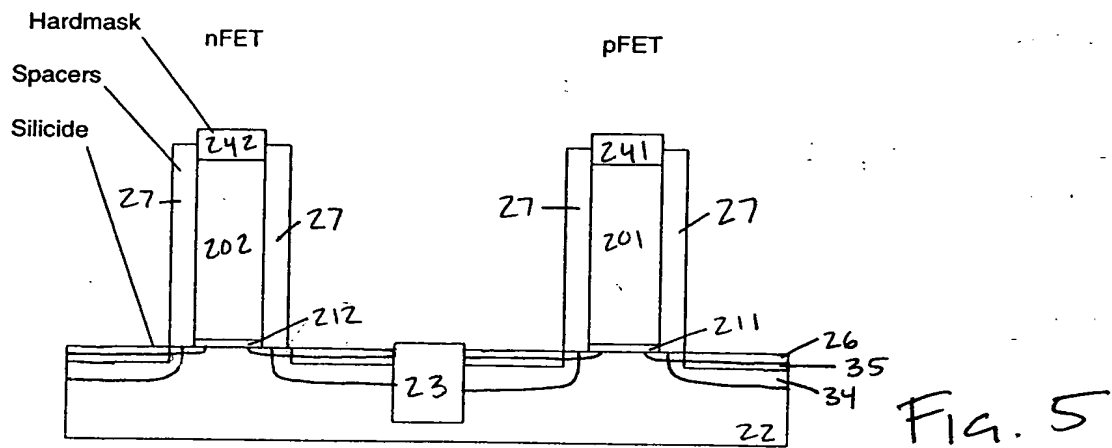


Fig. 4

Extension implants can be done prior to spacer formation. After the extensions are implanted, the source drain implants are performed followed by junction anneal and Silicide. The structure appears as shown below:



At this point in the process flow, an oxide film is deposited followed by CMP to the top of the gatestack.

CMP to top of gate stack

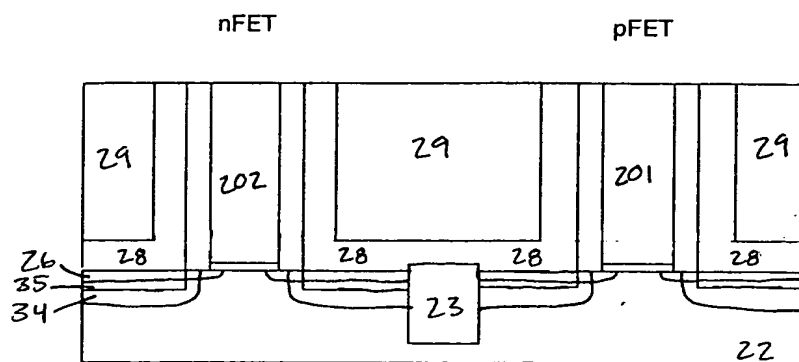


FIG. 7

An oxide or nitride film is patterned using a photolithography and etch process to block the nFET regions during pFET silicidation. The intermediate structure is shown below:

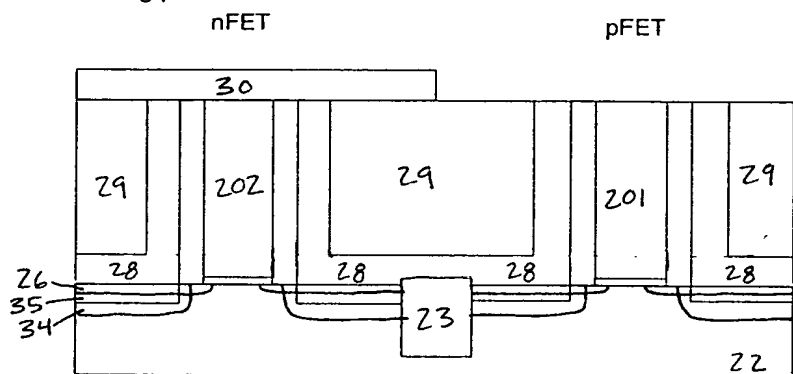
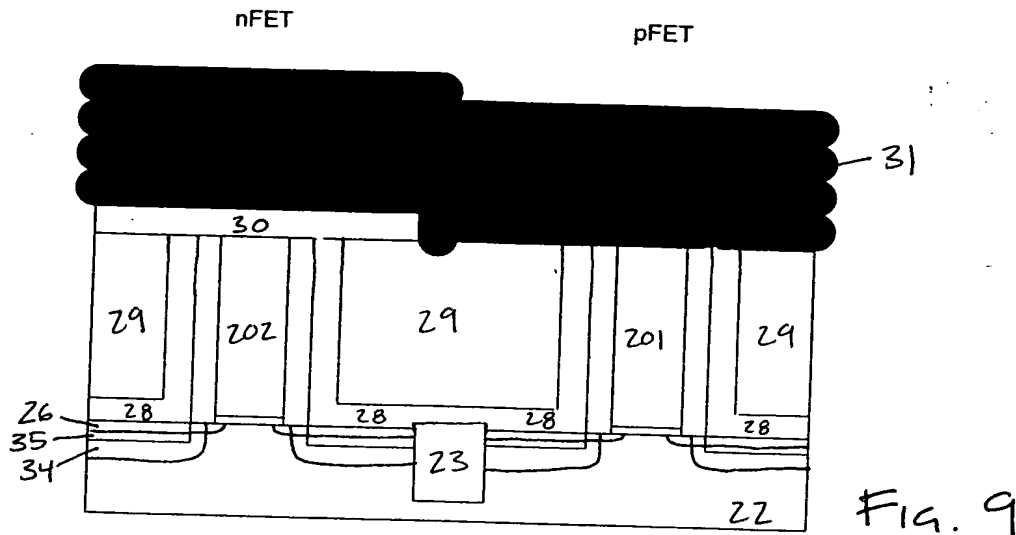


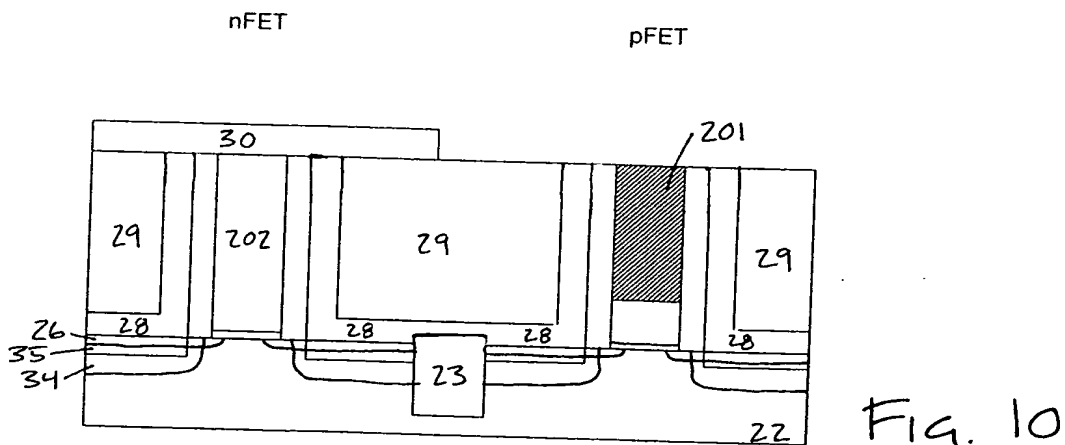
FIG. 8

Next, the metal to form the tensile silicide is deposited on the entire wafer as shown below:

Deposit Metal 1



The first silicide is reacted using a standard RTA process. After removing the excess unreacted metal, the structure is as follows:

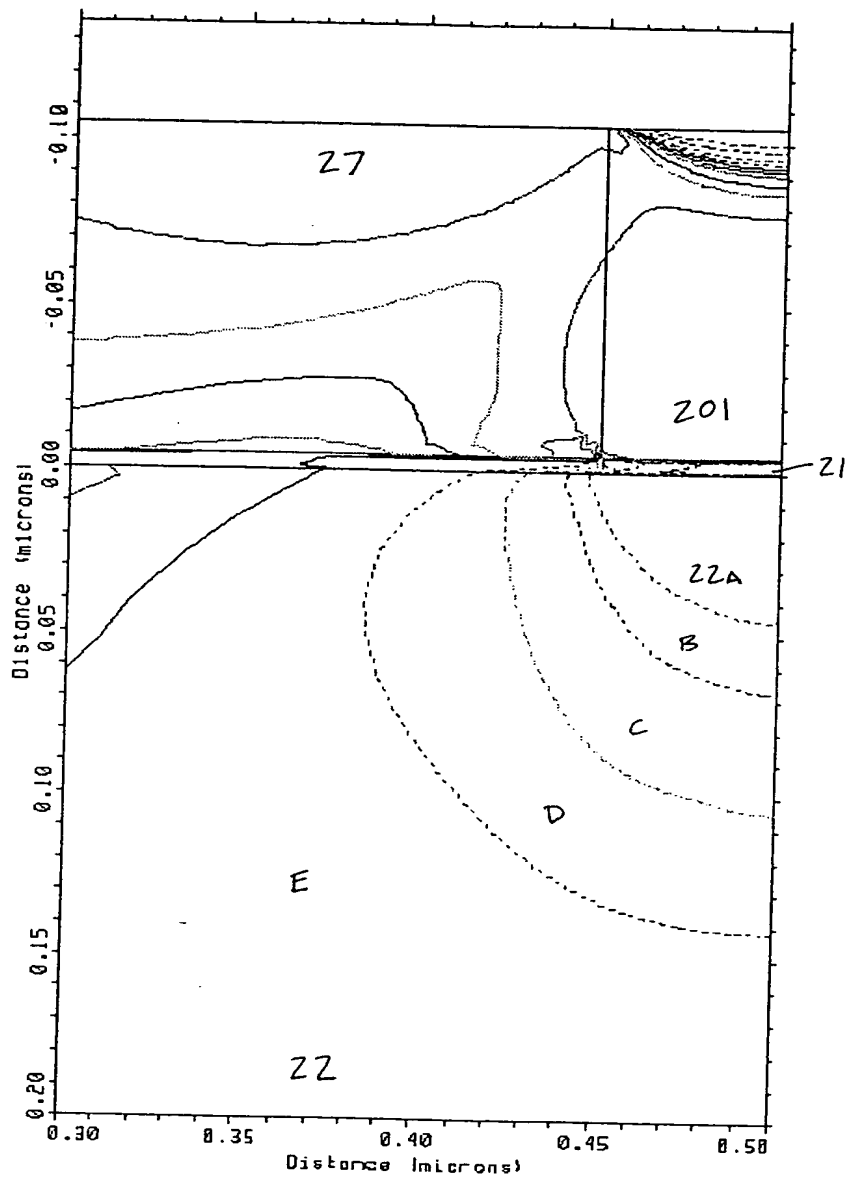


After the blocking layer for the nFET is removed using a dry or wet etching process, another blocking layer is applied in a manner similar to the first silicide to prevent metal from contacting the pFET gate while allowing the metal to contact the nFET gate. After depositing the metal to form the compressive silicide, the structure is as follows:

Any combination of these silicides and thicknesses may be used to optimize stress and therefore channel

FIG. 13

Cobalt silicide



Compressive PdSi (dashed lines) causes tension (solid lines) under the gate.

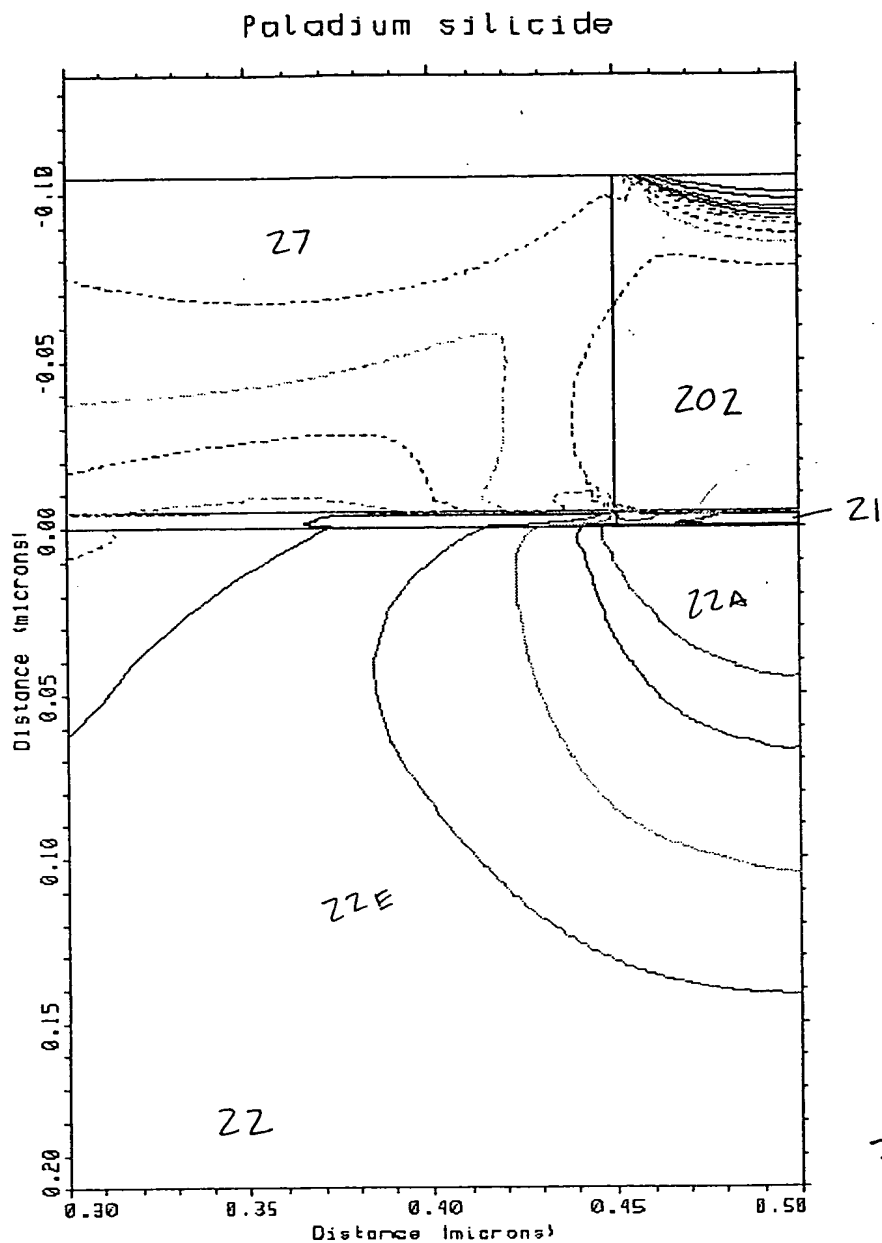


Fig. 14

## Invention:

The process flow is shown below to form independent silicide for the pFET and nFET. A tensile silicide like  $\text{CoSi}_2$  for example or  $\text{NiSi}$  is used for the pFET to impart compressive stress in the channel. The silicide for the nFET is a compressive silicide like palladium (or platinum) silicide for the purpose of imparting tensile stress in the channel.



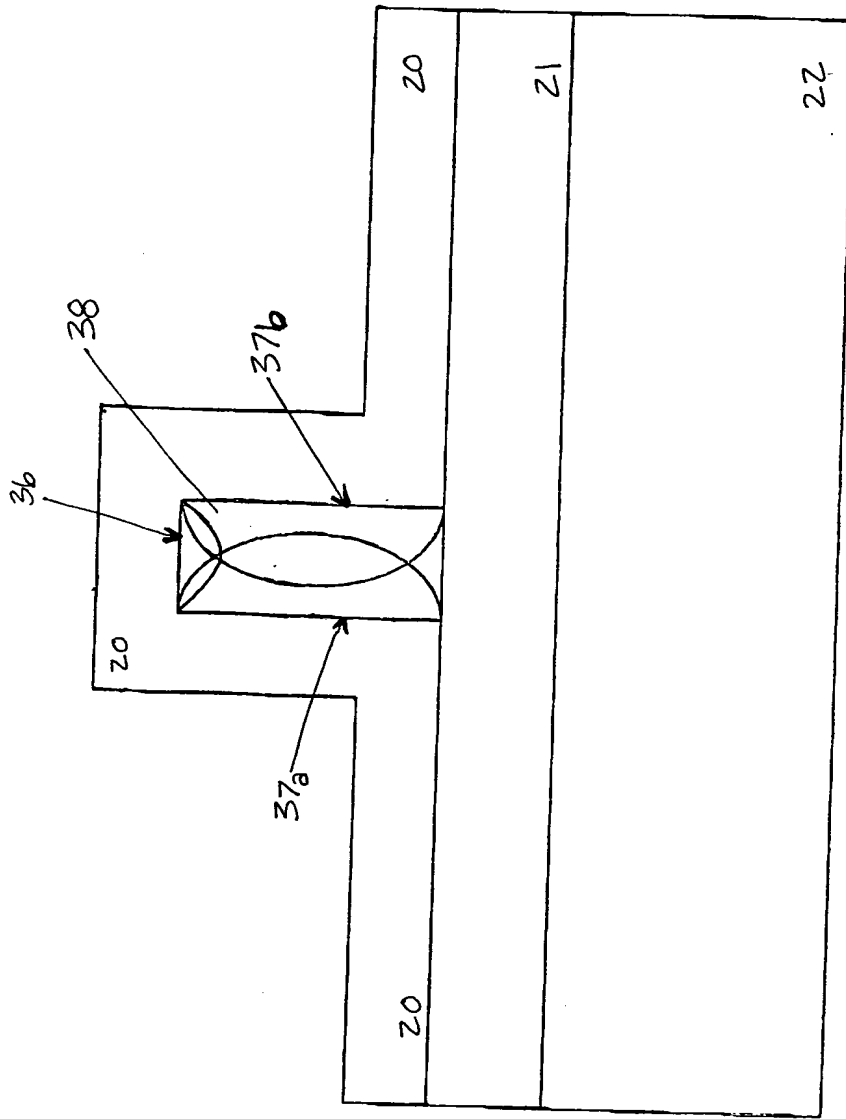


FIG. 15